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Combinational Circuits

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For

MCA/BCA /PGDCA Students of IGNOU

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Reference Material of IGNOU

Block 1 Unit 3
of
MCS-012

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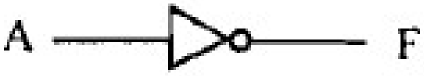
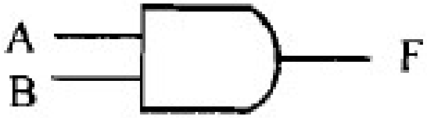
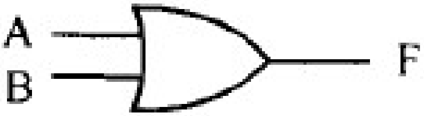
Outline of Presentation

- Logic Gates
- Combinational Circuits
- Introduction to Circuit Design - K-Maps
- Drawing Circuits
- ADDER circuit

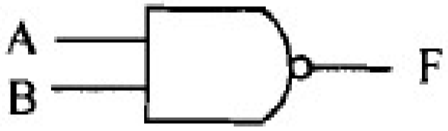
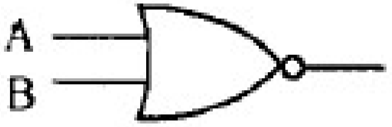
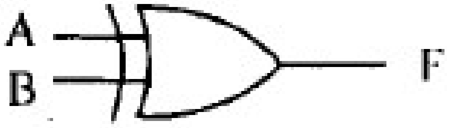
The Basic Logic Gates

Name	Graphic Symbol	Algebraic function	Truth Table
NOT		$F=\overline{A}$ or F= A	A F 0 1 1 0

AND		F= A.B
		or
		F = AB
			A B F
			0 0 0
			0 1 0
			1 0 0
			1 1 1

OR		F= A + B	A B F 0 0 0 0 1 1 1 0 1 1 1 1

Logic Gates

NAND		$F = \overline{A.B}$	A B F 0 0 1 0 1 1 1 0 1 1 1 0
NOR		$F = \overline{A + B}$	A B F 0 0 1 0 1 0 1 0 0 1 1 0
Exclusive-OR (XOR)		$F = A\overline{B} + \overline{A}B$ $F = A \oplus B$	A B F 0 -0 0 0 1 1 1 0 1 1 1 0

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Combinational Circuits

- Used to design basic functional units of a computer
- Gates are interconnected to produce a desired output from its input
- Can be expressed by a truth table or a Boolean function

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Combinational Circuit Design Issues

- The depth, number of gates in a sequence, should not exceed a specific level.
  - Reason: The output should be obtained with change in Input
- Fan in, i.e. number of input lines to ONE gate, and Fan out, i.e. number of gates to which output of ONE gate is fed, are limited by the power constraints.

Canonical and Standard Forms

Sum of Products (SOP)

- Minterm: Is a term of SOP expression, such that every variable of function is a part of the term in true or complement form.
- In F (A, B, C) = (A'. B.C') + (A . B') ONLY A'.B.C' is minterm.
- the term A'.B.C' will be one only if A' = 1 (A=0), B = 1and C' = 1 (C=0), for any other combination of values of A, B, C the minterm A'.B.C' will have 0 value.

Canonical and Standard Forms

Product of Sums (POS)

- Maxterm: is a term of POS expression, such that every variable of function is a part of term in true or complemented form.
- In F (A, B, C) = (A + B’ + C). (A+B’) maxterm is (A + B’ +C).
- The maxterm A+B’+C will has 0 value only for A = 0, B’ = 0 (or B=1) and C = 0 for all other combination of values of A, B, C it will have a value 1.

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Introduction to Circuit Design

- Algebraic Simplification
- Karnaugh Maps
- Quine McCluskey Method

- We will use Kanaugh Maps to show the process of Design.

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Problem 1

- Assume that you are asked to design a circuit that accepts four bits as input and generates an output 1 if the input is an Even Number; else produces an output 0.

Step 1: The Truth Table

Decimal	A	B	C	D	Output
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	1
7	0	1	1	1	0

Step 1: The Truth Table

Decimal	A	B	C	D	Output
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	0
12	1	1	0	0	1
13	1	1	0	1	0
14	1	1	1	0	1
15	1	1	1	1	0

The K-map for Even Numbers

\CD AB \	00	01	11	10
00	0	1	3	2 1
01	4 1	5	7	6 1
11	12 1	13	15	14 1
10	8 1	9	11	10 1

Adjacency 1: CD'

\CD AB \	00	01	11	10
00	0	1	3	2 1
01	4 1	5	7	6 1
11	12 1	13	15	14 1
10	8 1	9	11	10 1

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Adjacency 2: A D’

\CD AB \	00	01	11	10
00	0	1	3	2 1
01	4 1	5	7	6 1
11	12 1	13	15	14 1
10	8 1	9	11	10 1

Adjacency 3: B D'

\CD AB \	00	01	11	10
00	0	1	3	2 1
01	4 1	5	7	6 1
11	12 1	13	15	14 1
10	8 1	9	11	10 1

F= CD’ + A D’ + B D’

\CD AB \	00	01	11	10
00	0	1	3	2 1
01	4 1	5	7	6 1
11	12 1	13	15	14 1
10	8 1	9	11	10 1

Problem 2

- Assume that you are asked to design a circuit that accepts four bits as input and generates an output 1 if the input is a Prime Number; else produces an output 0.

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Step 1: The Truth Table

Decimal	A	B	C	D	Output
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	1

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Step 1: The Truth Table

Decimal	A	B	C	D	Output
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	0

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The K-map for Prime Numbers

\CD AB \	00	01	11	10
00	0	1	3 1	2 1
01	4	5 1	7 1	6
11	12	13 1	15	14
10	8	9	11 1	10

Adjacency 1 & 2:

A’B’C + BC’D

\CD AB \	00	01	11	10
00	0	1	3 1	2 1
01	4	5 1	7 1	6
11	12	13 1	15	14
10	8	9	11 1	10

Adjacency 3 and 4:

A’CD + B’CD

\CD AB \	00	01	11	10
00	0	1	3 1	2 1
01	4	5 1	7 1	6
11	12	13 1	15	14
10	8	9	11 1	10

$F=A'B'C + BC'D +$ $A'CD + B'CD$

\CD AB \	00	01	11	10
00	0	1	3 1	2 1
01	4	5 1	7 1	6
11	12	13 1	15	14
10	8	9	11 1	10

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The K-map for Prime Numbers – Upto Value 9

\CD AB \	00	01	11	10
00	0	1	3 1	2 1
01	4	5 1	7 1	6
11	12 X	13 X	15 X	14 X
10	8	9	11 X	10 X

F= BD + B’C

Use of DONOT CARE condition

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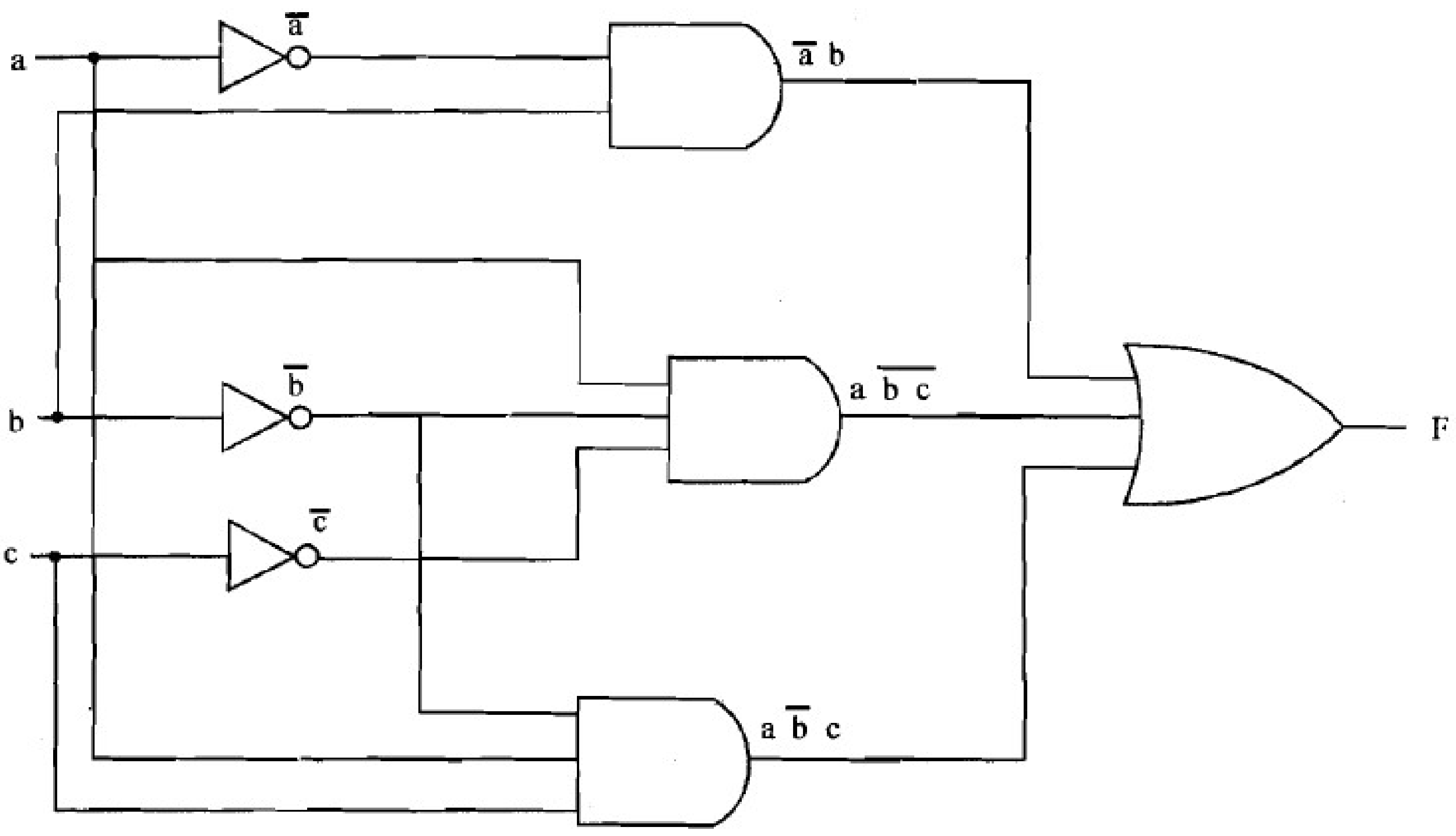
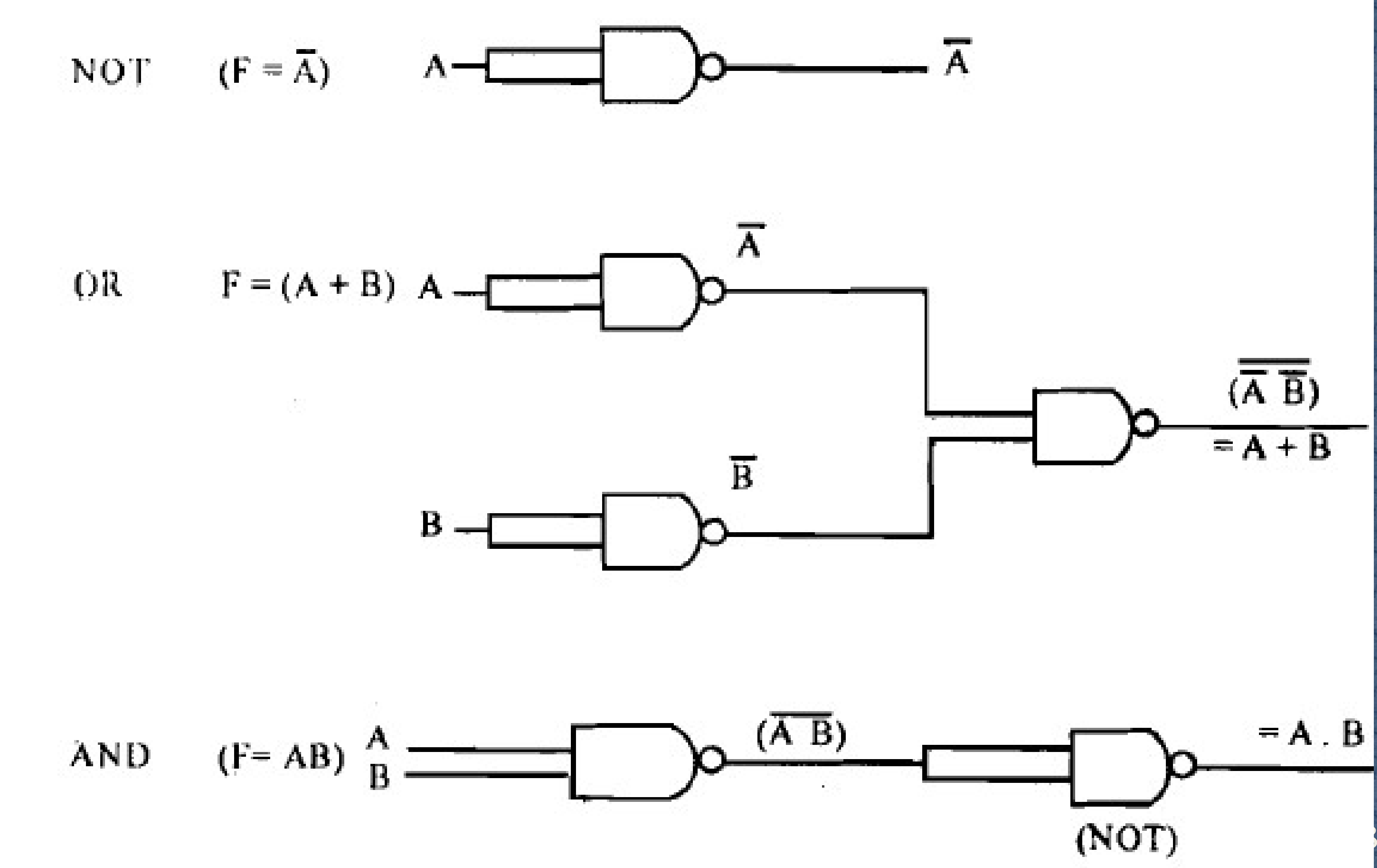
Drawing Circuits



(a) $F - a\bar{b}\bar{c} + a\bar{b}c \mid \bar{a}b$

Functionally Complete Set of Gates: NAND



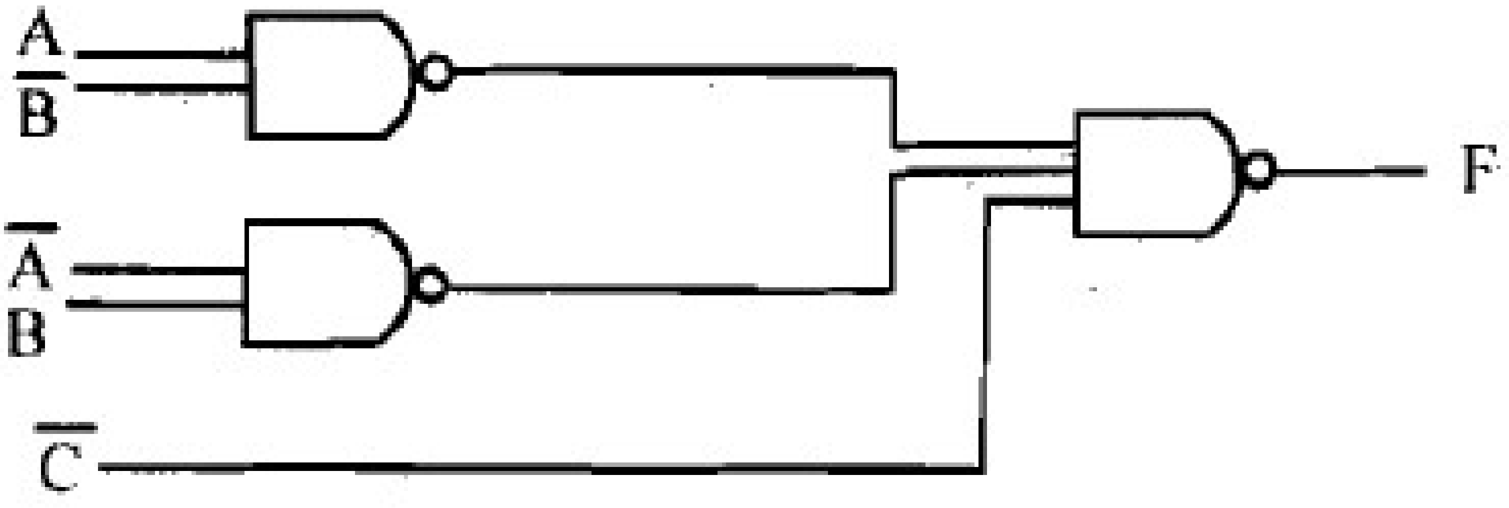
$F(A,B,C) = \sum(1,2,3,4,5,7)$

\BC A \	00	01	11	10
0	0	1 1	3 1	2 1
1	4 1	5 1	7 1	6

- F= C + A B’ + A’ B
- F= [(C + AB’ + A’B)’]’
- F= [C’ . (AB’)’ . (A’B)’]’ DeMorgan’s Law (A+B)’ = A’.B’
- F== NAND of (NAND C; NAND AB’;
  NAND A’B);

The Function

- F= C + A B’ + A’ B
- F== NAND of (NAND C; NAND AB’; NAND A’B);



(b) Logic circuit using NAND only

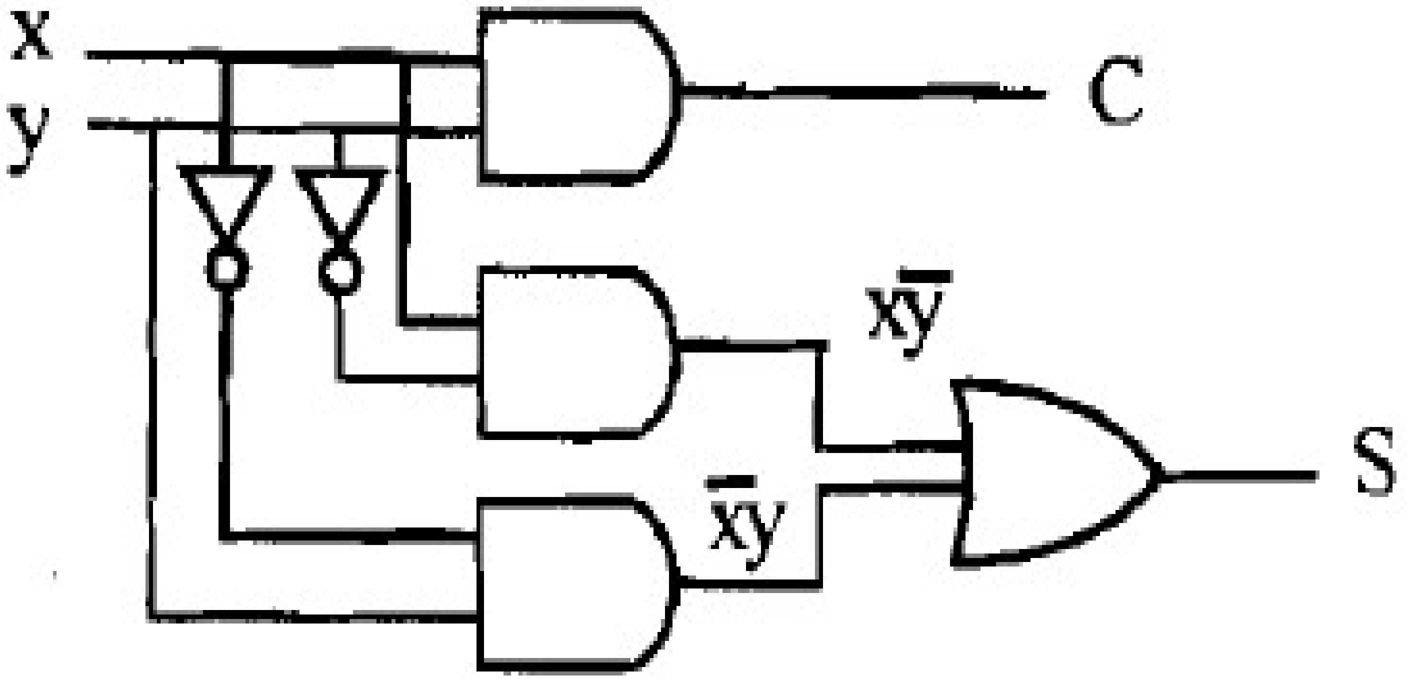
Half Adder:
Adding two bits

- **Truth table: (Draw 2 K-maps 1 each for Sum bit and Carry bit respectively)**

Decimal	A	B	Sum bit	Carry bit
0	0	0	0	0
1	0	1	1	0
2	1	0	1	0
3	1	1	0	1

Half Adder Circuit

- C=A B   and S = A B’ + A’ B



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Full Adder:
Adding three bits

Decimal	A	B	Carry in	Sum bit	Carry bit
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

K-Map for Full Adder

\BC A \	00	01	11	10
0	0	1 1	3	2 1
1	4 1	5	7 1	6

Sum=A’B’C+A’BC’+AB’C’+ABC

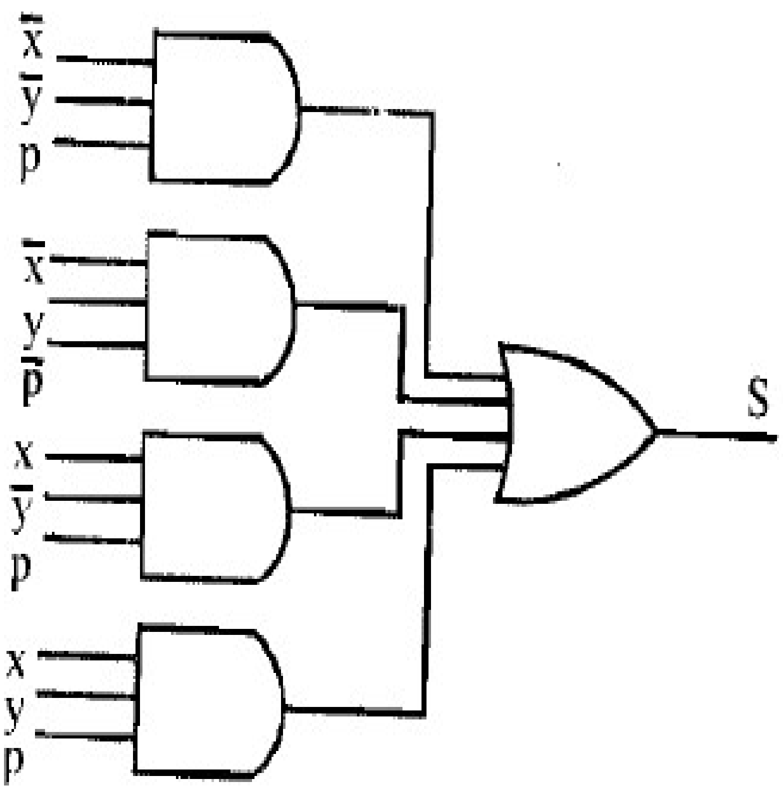
\BC A \	00	01	11	10
0	0	1	3 1	2
1	4	5 1	7 1	6 1

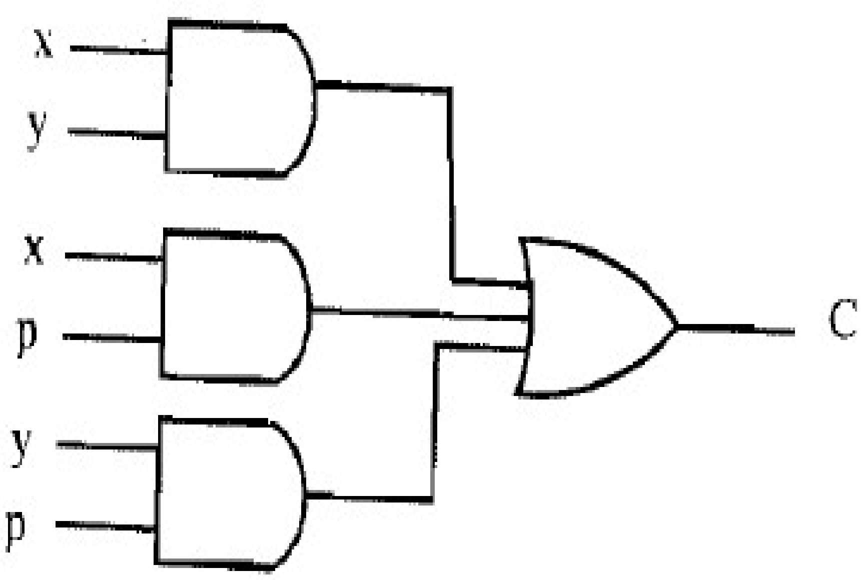
Carry = BC+AC+AB

Full Address Circuit

Sum=A’B’C+A’BC’+AB’C’+ABC

Carry = BC+AC+AB

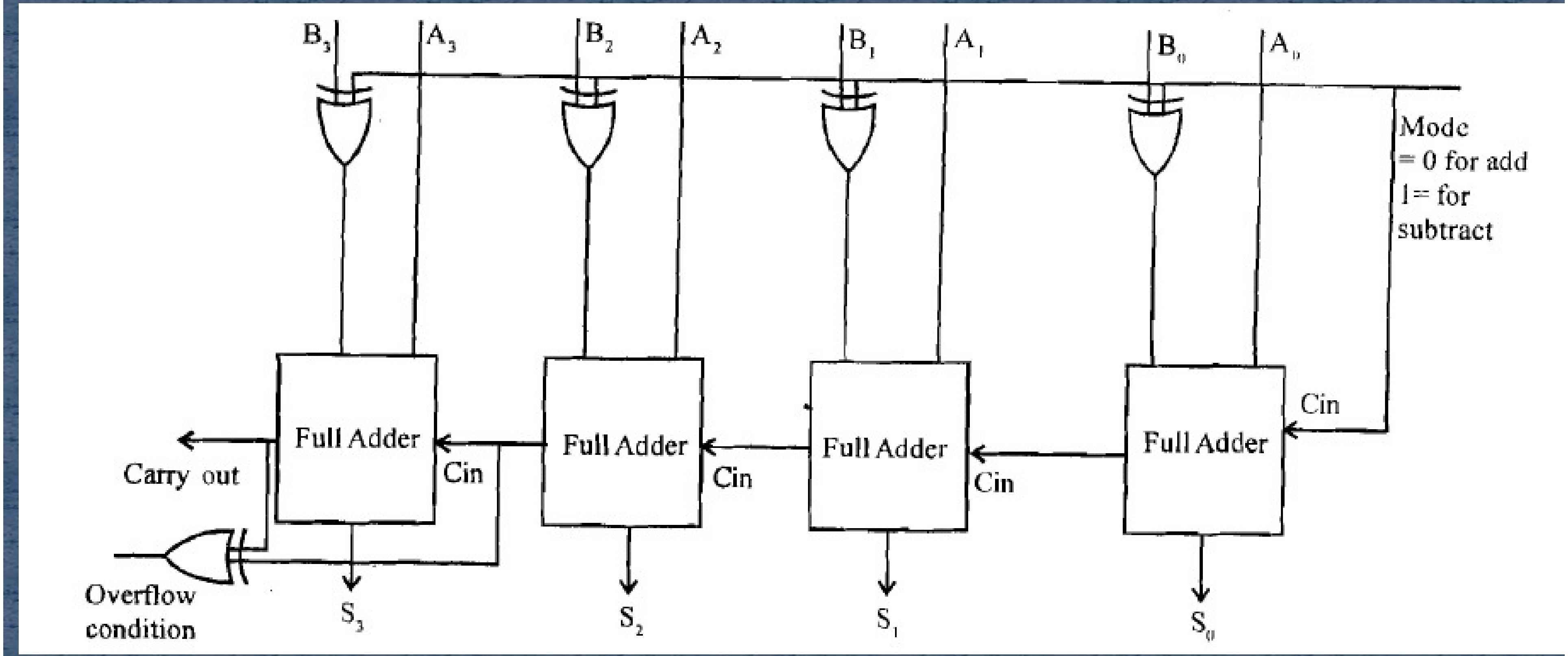




Adder-Subtractor Circuit

$A_3\,A_2\,A_1\,A_0$ 1010 M=0 $B_3\,B_2\,B_1\,B_0$ 0101 Cin =0

$A_3\,A_2\,A_1\,A_0$ 1010 M=1 input($B_3\,B_2\,B_1\,B_0$) 1010 Cin =1



Check Your Progress

- Study and draw all the circuits of the Block 1 Unit 3 and solve all the problems given in your Block.