Sequential Circuits

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For

MCA/BCA /PGDCA Students of IGNOU

Reference Material of IGNOU

Block 1 Unit 4 of MCS-012

Outline of Presentation

- Sequential Circuits
- Flip-Flops
- Some Sequential Circuits

Sequential Circuits: The Definition

- A circuit whose output is dependent on the Input and Current State of the Circuit
- An interconnection of
  - combinational circuits and
  - storage elements
- The storage elements, called flip-flops, store binary information that indicates the state of sequential circuit at that time

Why Needed?

- Useful for cases
  - where a series of events occur
  - Storage of past information is useful
- For example – Counters

Classification of Sequential Circuits

- Broadly classified, depending upon the time at which their internal state change
  - Synchronous: The state changes at Discrete Intervals.
    - Use flip-flops
    - A good choice for discrete digital devices
  - Asynchronous sequential circuits may be regarded as combinational circuit with feedback

Synchronization in a sequential circuit

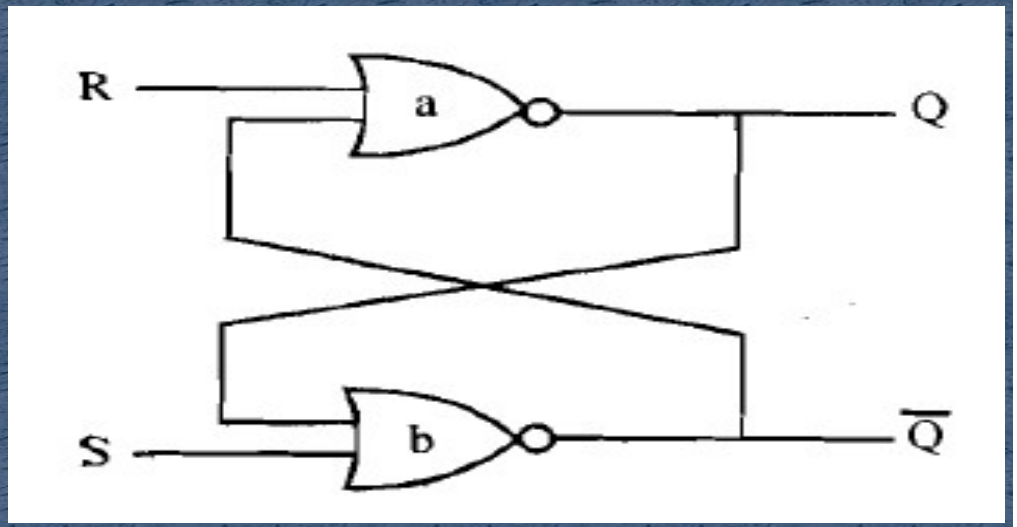
- The synchronization in a sequential circuit is achieved by a clock pulse generator, which gives continuous clock pulse.
- A clock pulse can have two states: 0 or 1; disabled or active state. The storage elements can change their state either when a clock pulse occurs or during the rising or falling edge of the clock pulse.

Flip-Flops

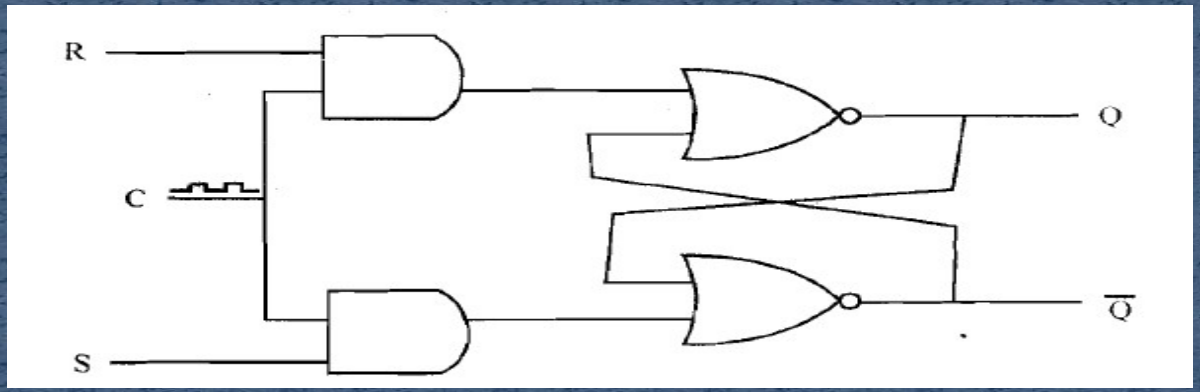
- A flip-flop is a binary cell, which stores one bit of information. It itself is a sequential circuit.
- Flip-flop can change its state when clock pulse occurs but when?
  - Generally, a flip-flop can change its state when the clocks transitions from 0 to 1 (rising edge) or from 1 to 0 (falling edge) and not when clock is 1
  - If the storage element changes its state when clock is exactly at 1 then it is called a latch.
  - A flip-flop is edge-triggered and latch is level-triggered.

An S-R Latch using NOR gates

- Can be constructed using NOR or NAND gates
- Two Input – S (SET) and R (RESET)
- Output –If Q=1 & Q'=0, the latch is in the SET state
- If Q=0 & Q'=1, it is the RESET state.

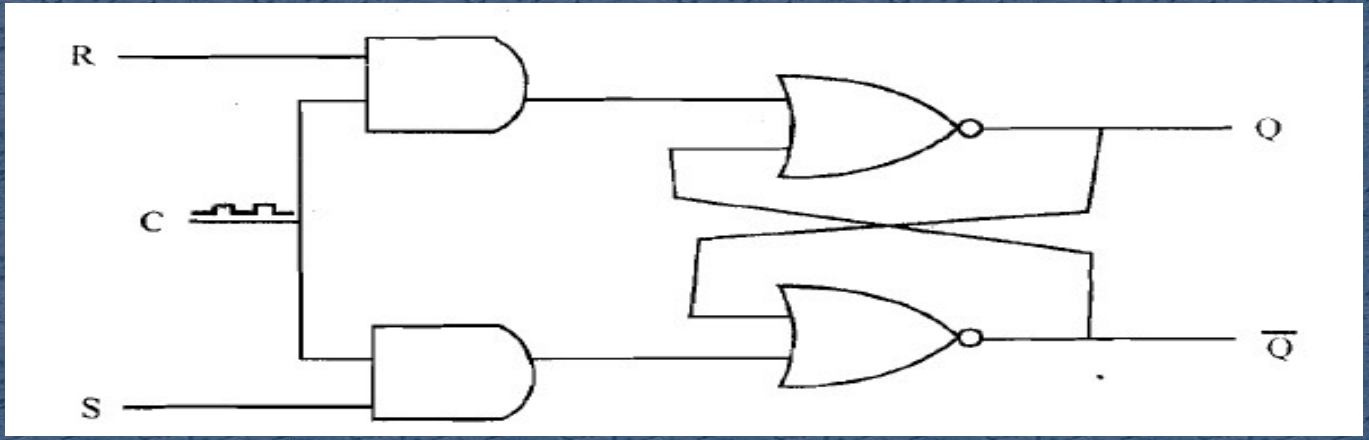


S R Flip-flop



S	R	Q	Q’
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0



Characteristic Table

C	S	R	Q(T+1)
1	0	0	Q(T) No change in state
1	0	1	0 Reset
1	1	0	1 Set
1	1	1	x undefined

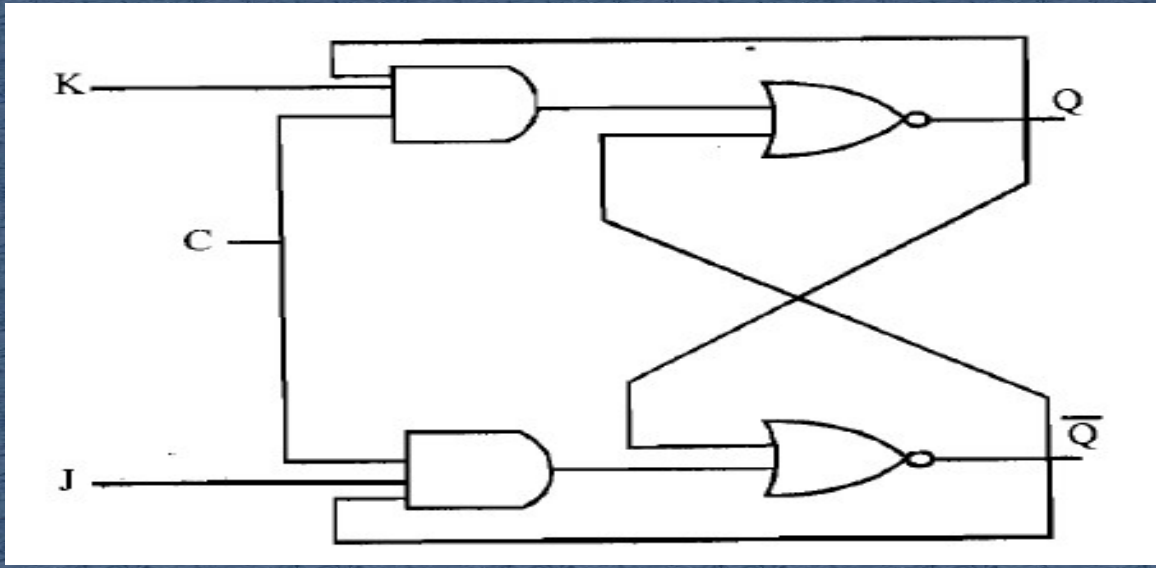
Summary of S-R Flip-flops Operations

- If no clock signal i.e. C=0
  - No change in OUTPUT irrespective of R & S values
- Occurrence of Clock Signal
  - When S=0, R=0 then output Remains Unchanged
  - When R=1 S=0 then output Q=0 & Q'=1 (Reset)
  - When S=1, R=0 then output Q=1 & Q'=0 (Set)
  - When R=1 S=1 then output is not defined
    - May become 0 or 1 depending upon internal timing delays of circuit.

J-K Flip-flop

- The J-K flip-flop
  - Modification of S-R flip-flop
  - Two input J and K, identical to S and R
  - When J & K both are 1, the flip- flop output is complemented with clock transition.

A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0



Characteristic Table

C	J	K	Q(T+1)
1	0	0	Q(T) No change in state
1	0	1	0 Reset
1	1	0	1 Set
1	1	1	Complement Q(T)

Excitation Tables

- The characteristic tables of flip-flops –
  - provide the information of next state based on present state and input values
  - Such tables are useful for analysis of sequential circuits.
- For circuit design: NEED to define the FLIP-FLOP input, for the required transition from a given state to next state – called Excitation Table of flip-flop

How to Make Excitation Table for J-K Flip flop?

Transition from present state 0 to next state 0:

a) **J=0, K=0, No change in the state of flip flop**

b) **J=0, K=1, Reset flip-flop to state 0**

Thus J=0 but K can be 0 or 1 that is X.

Characteristic Table

C	J	K	Q(T+1)
1	0	0	Q(T) No change in state
1	0	1	0 Reset
1	1	0	1 Set
1	1	1	Complement Q(T)

Transition from present state 0 to next state 1:

a) J=1, K=0, Set flip flop state to 1

b) J=1, K=1, Complement flip-flop from 0 to 1

Thus J=1 but K can be 0 or 1 that is X.

Characteristic Table

C	J	K	Q(T+1)
1	0	0	Q(T) No change in state
1	0	1	0 Reset
1	1	0	1 Set
1	1	1	Complement Q(T)

Transition from present state 1 to next state 0:

a) J=0, K=1, Reset the flip flop state to 0

b) J=1, K=1, Complement flip-flop from 1 to 0

Thus J can be 0 or 1 that is X, but K=1.

Characteristic Table

C	J	K	Q(T+1)
1	0	0	Q(T) No change in state
1	0	1	0 Reset
1	1	0	1 Set
1	1	1	Complement Q(T)

Transition from present state 1 to next state 1:

a) J=0, K=0, No change in state 1

b) J=1, K=0, Set flip flop state to 1

Thus, J can be 0 or 1 that is X, but K=0

Characteristic Table

C	J	K	Q(T+1)
1	0	0	Q(T) No change in state
1	0	1	0 Reset
1	1	0	1 Set
1	1	1	Complement Q(T)

Summary of the process

Present State	Next State	J	K	Can be achieved by
0	0	0	X	a) J=0, K=0, No Change b) J=0, K=1, Reset
0	1	1	X	a) J=1, K=0, Set b) J=1, K=1, Complement
1	0	X	1	a) J=0, K=1, Reset b) J=1, K=1, Complement
1	1	X	0	a) J=0, K=0, No Change b) J=1, K=0, Set

Excitation Tables for J-K Flip Flop

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

The symbol X in the table means
don't care condition i.e.
doesn't matter whether input is 0 or 1

Design of a Sequential Circuit

- Counter:
  - A fundamental circuit used for timing and control
- Problem: Design a 2 bit counter, that changes its input when an external input X is 1.
- For the present design we are using D flip flop.
- For 2 bit counter, 2 flip-flops are needed

Characteristics table and Excitation table for D flip-flop

D	Q(t+1)
0	0 Clear
1	1 Set

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

The Change of State

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

Present State		Input	Next State		Input to Flip Flops	
A	B	X	A	B	D_A	D_B
0	0	0	0	0		
0	0	1	0	1		
0	1	0	0	1		
0	1	1	1	0		
1	0	0	1	0		
1	0	1	1	1		
1	1	0	1	1		
1	1	1	0	0		

The Change of State

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

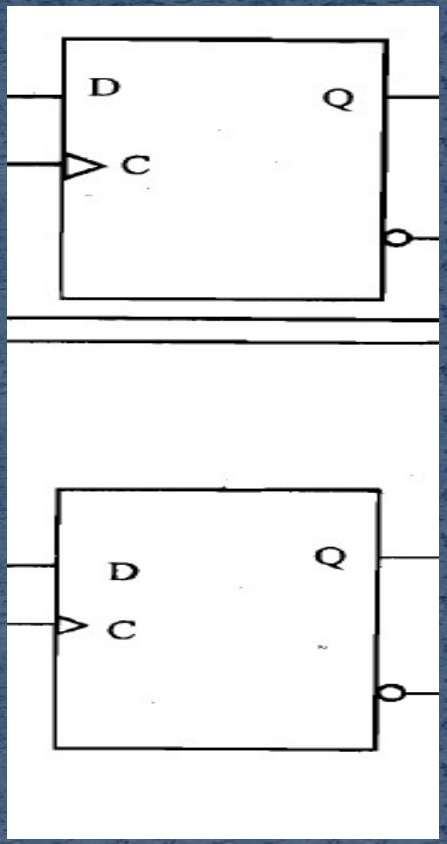
Present State		Input	Next State		Input to Flip Flops	
A	B	X	A	B	D_A	D_B
0	0	0	0	0	0	
0	0	1	0	1	0	
0	1	0	0	1	0	
0	1	1	1	0	1	
1	0	0	1	0	1	
1	0	1	1	1	1	
1	1	0	1	1	1	
1	1	1	0	0	0	

The Change of State

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

Present State		Input	Next State		Input to Flip Flops	
A	B	X	A	B	D_A	D_B
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	1	0	1
0	1	1	1	0	1	0
1	0	0	1	0	1	0
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	0	0	0	0

What is required?



How to Design Circuit?

INPUT			OUTPUT	
Present State		Input	Input to Flip Flops	
A	B	X	D_A	D_B
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

K-map for D_A and D_B

Present State		Input	Input to Flip Flops	
A	B	X	D_A	D_B
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

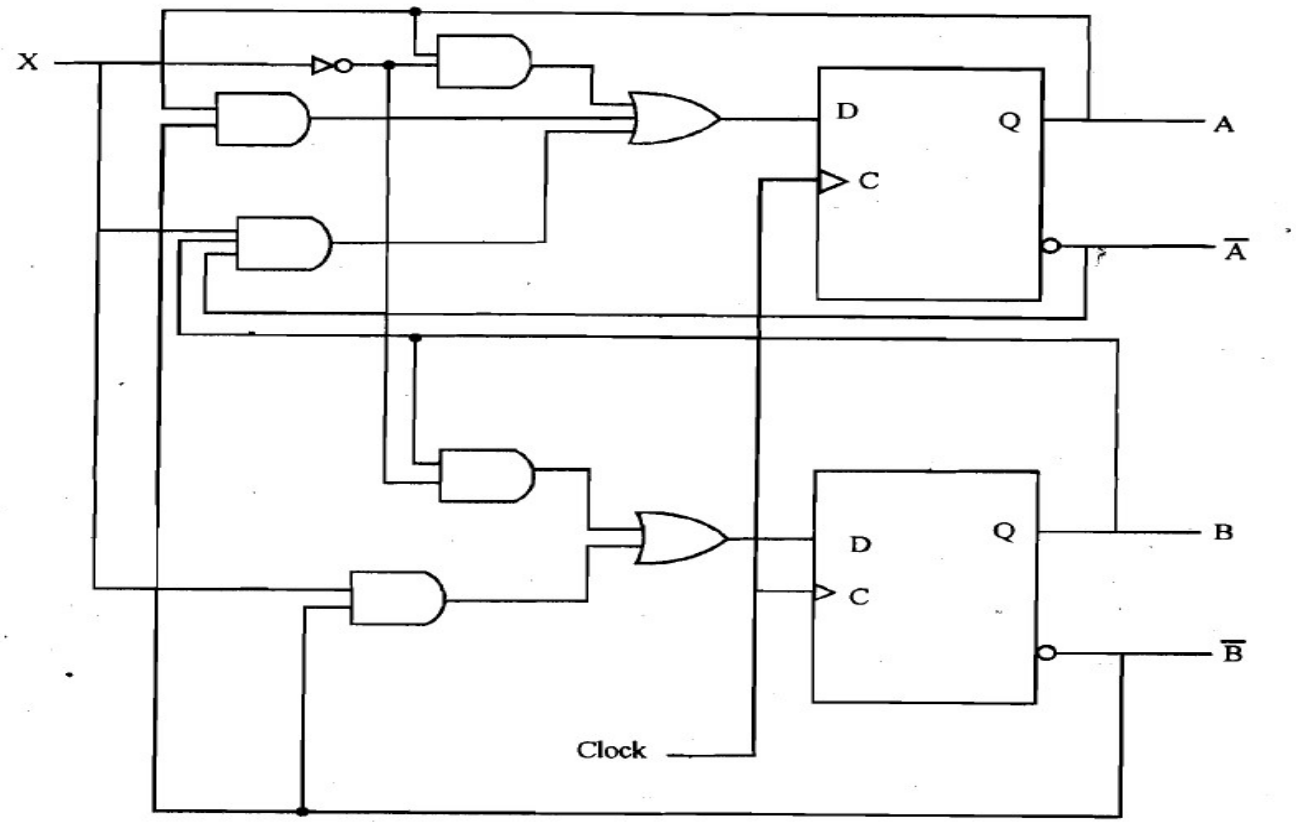
A\BX	00	01	11	10
0	0	1	3 1	2
1	4 1	5 1	7	6 1

For D_A: F=AB'+AX'+A'BX

A\BX	00	01	11	10
0	0	1 1	3	2 1
1	4	5 1	7	6 1

For D_B: F=B'X+BX'

The Counter Circuit



Check Your Progress

- Attempt all the Questions given in CYP of your Block
- Read the functioning of all the Sequential Circuits